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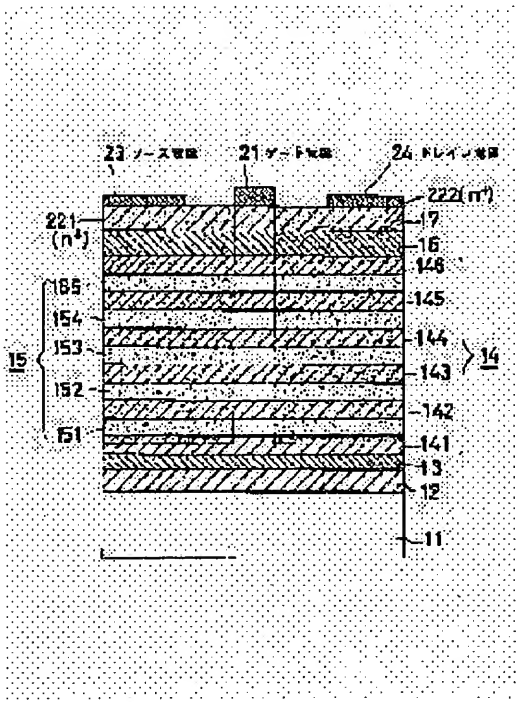
(54) COMPOUND SEMICONDUCTOR DEVICE

(57)Abstract:

PURPOSE: To provide a compound semiconductor device capable of constituting a transistor, which undergoes no change in characteristics, such as an electron mobility and the like, in a wide temperature range and is suitable for a high- speed and high-frequency circuit.

CONSTITUTION: An I-type GaAs buffer layer 12 and an I-type AlGaAs barrier layer 13 are formed on a semi-insulative GaAs single crystal substrate 11 and a multilayer structure obtainable by forming alternately I-type GaAs layers 141 to 146 and delta doped-layers 151 to 155, which are constituted by doping Si to the surfaces of these layers 141 to 146, on the layer 13 is formed. Moreover, a barrier layer 16 and a cap layer 17 are formed on the multilayer structure and after a gate electrode 21 is formed, n+ layers 221 and 222 are formed by implanting an impurity and a source electrode 23 and a drain electrode 24 are formed, whereby field-effect transistor is constituted.



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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the compound semiconductor equipment which properties, such as electron mobility, are stabilized in a large temperature region, and was set up especially.
[0002]
[Description of the Prior Art] Ga As In the high-speed logic IC constituted using the field effect transistor, it is known that it is that to which the upper limit of the working speed of this IC becomes later than the speed limit calculated from the switching rate of the transistor which constitutes this IC.
[0003] The cause by which the working speed of this IC becomes slow is because the current serviceability of the field effect transistor which constitutes IC is small, and is because the rate which discharges the input capacitance of the transistor of the next step and the stray capacity of wiring used as the load of a transistor becomes slower than the switching rate of a transistor.
[0004] In order to solve such a problem, it is necessary to heighten the load-carrying-capacity actuation capacity of a transistor. For this reason, it is necessary to raise the carrier (for it to be [in the case of the field effect transistor of N channel] electron hole in the case of electron and field effect transistor of P channels) concentration of the active layer of a transistor. Here, it is Ga As. It is known for the delta dope structure which doped the impurity atom to one atomic layer in the compound semiconductor equipment of a system that high carrier concentration will be obtained.
[0005] In the transistor of delta dope structure, the delta dope layer is set as the range of about 10-100nm from the front face. With such structure, the temperature characteristic of the mobility of a carrier changes with the amounts of dopes of an impurity a lot. Therefore, carrier concentration and mobility come to be uniquely decided by the small conditions of the temperature dependence of mobility, and the engine performance cannot be raised on them.
[0006]
[Problem(s) to be Solved by the Invention] This invention was made in view of the above points, tends to improve the mutual conductance of a transistor which has especially delta dope structure, and the temperature dependence of a threshold electrical potential difference, and tends to offer compound semiconductor equipment applicable to the high speed and RF circuit which do not have change in transistor characteristics, such as electron mobility, over a large temperature requirement.
[0007]
[Means for Solving the Problem] The compound semiconductor equipment concerning this invention is Ga As. It is what forms a multilayer-structure layer through a buffer layer on the semi-conductor substrate which becomes with a single crystal. This multilayer-structure layer is what carried out the laminating of the base material semi-conductor layer made into one unit, and constituted it. In 1 atomic layer of this semi-conductor layer, an atom of a different kind is doped and a dope layer is formed at the laminating interface of each of this base material semi-conductor layer, and it is made to carry out two or more step laminating so that two-layer formation of this dope layer may be carried out at least.

[0008]
[Function] Thus, since it is the thing the number of is not one, forms the two or more layers delta dope layer which doped and formed the heteroatom in the compound semiconductor equipment constituted, and he is trying to constitute a multilayer-structure layer, the temperature dependence of electron mobility is improved and it has the outstanding description which can set the concentration of a carrier now as a desired value according to the object of a transistor.
[0009]
[Example] Hereafter, one example of this invention is explained with reference to a drawing. Drawing 1 shows the cross-section structure of the field effect transistor constituted by the epitaxial growth substrate, and explains the structure of this epitaxial growth substrate according to that production process first.
[0010] although epitaxial growth is what is formed by molecular beam epitaxy (MBE law) here -- MOCVD -- if it is the means in which growth control of atomic layer order, such as law (method of organic metal vapor growth), is possible, it is usable suitably.
[0011] First, half-insulation Ga As i-Ga As which prepares the single crystal substrate 11 of a semi-conductor, and does not dope an impurity on this single crystal substrate 11 The buffer layer 12 to depend is formed with epitaxial growth by 0.5 micrometers in thickness.
[0012] Thus, if a buffer layer 12 grows, a barrier layer 13 is formed by 300nm in thickness on this buffer layer 12, and this barrier layer 13 is aluminum0.3 Ga 0.7 As. It is constituted.
[0013] i-Ga As which does not dope an impurity on this barrier layer 13 Layer 141 Ga currently opened for this growth after making it grow up by 6nm in thickness It is Si after closing, this and coincidence, or several seconds about the shutter of an evaporation source. They are an aperture and Si for 60 seconds about the shutter of an evaporation source. Doping layer 151 It forms and one delta dope layer is formed.
[0014] Next, it is this Si again. It is Ga while closing the shutter of an evaporation source. The shutter of an evaporation source is opened and it is i-Ga As. Layer 142 6nm is grown up and it is this Ga. It is Si after closing an evaporation source shutter. They are an aperture and Si for 60 seconds about the shutter of an evaporation source. Doping layer 152 It forms. i-Ga As which does not dope an impurity by repeating such a process 5 times Layer 141-145 (14) and Si Doping layer 151-155 The multilayer structure which has arranged (15) by turns is formed, and it is i-Ga As further to the last. Layer 146 It forms and this multilayer-structure layer is completed.
[0015] That is, this multilayer-structure layer is i-Ga As used as one unit. It is carrying out the laminating, using a layer as a base material semi-conductor layer, in the laminating interface of this base material semi-conductor layer, at least, a heteroatom is doped, it comes to form a doping layer (delta dope layer) in 1 atomic layer, and five stratification of this delta dope layer is carried out for this base material semi-conductor layer.
[0016] On such the multilayer-structure section, it is i-aluminum 0.3 Ga0.7 As. A barrier layer 16 (barrier layer) is formed by the thickness of 30nm, and it is i-Ga As to the last. The cap layer 17 is formed and this epitaxial growth substrate is completed.
[0017] The gate electrode 21 is first formed by constituting a field effect transistor using such an epitaxial growth substrate by forming the thin film of WSi x (x= 0.6) by RF sputtering so that it may become 30nm in thickness, and carrying out pattern etching of this thin film by reactive ion etching the whole surface on the front face of an epitaxial growth substrate, i.e., the front face of the cap layer 17.
[0018] Thus, if the gate electrode 21 is formed, this gate electrode 12 will be used as a mask, and it is Si from the front face of the cap layer 17. Si which poured in ion, annealed for 5 seconds and was doped at 900 degrees C It is activated and the n+ layer 221 and 222 (field shown in drawing by the set of the point surrounded with the chain line) are formed.
[0019] And n+ layer 221 of the front face of the cap layer 17 And 222 The source electrode 23 and the drain electrode 24 are formed by forming in the corresponding source and a corresponding drain part by Au germanium 40nm and Au 150nm, and performing the sinter for 90 seconds into them at 450 degrees C.

[0020] Drawing 2 shows the temperature dependence of the electron mobility in the epitaxial growth substrate constituted as mentioned above. Electronic mobility comes to be settled in very narrow range called 2/Vs 1020-950cm in 77K-350K so that clearly from this drawing. Moreover, sheet carrier concentration is also larger than 2x1013cm-2 and the case where there is a delta dope layer.
[0021] The following [phenomenon / such] becomes a factor. First, sheet carrier concentration can be made into the multiple of the number of layers by making a delta dope layer into the multilayer more than two-layer from one layer. Therefore, spacing of this delta dope layer can be selected to a suitable value.
[0022] In an example, although the number of delta dope layers was set as five layers, if this number of layers becomes more than two-layer, the same effectiveness will be demonstrated. He can understand that temperature dependence is very small as compared with the case of one layer by drawing 3's comparing and showing the temperature dependence of the mobility in the case of being the case where there is a delta dope layer, and two-layer, and making a delta dope layer two-layer.
[0023] Although spacing of this delta dope layer was set to 6nm in the example, it is expectable that the same effectiveness will be demonstrated if it is less than 100nm, and the effectiveness of the formation of a two-dimensional phonon becomes remarkable, so that that spacing is narrow. Although the temperature dependence of sheet carrier concentration in case drawing 4 is the case where there is a delta dope layer, and two-layer is shown, required sheet carrier concentration can be attained by stratifying two or more number of delta dope layers.
[0024] aluminum Ga As of n mold Ga As which touches a layer and this At an interface with a layer, they are aluminum Ga As and Ga As. Band gaps (forbidden-band width of face) differ, and it is aluminum Ga As. The direction of a band gap is large. For this reason, an electron comes to move to the large Ga As side of an electron affinity from aluminum Ga As, and insulation becomes large, so that forbidden-band width of face is large.
[0025] If this is corresponded to an example, the Ga As layer 14 which contains a delta dope layer in drawing 1 is aluminum Ga As. It has structure pinched by layers 13 and 16. Therefore, aluminum Ga As with big forbidden-band width of face An electron stops easily being able to go into layer 13 and 16 side, and it is Ga As. It will be in the condition that the electron was confined in the layer 14 side. That is, sheet carrier concentration improves. Moreover, aluminum Ga As Since a layer 16 exists, the Schottky barrier becomes large and gate pressure-proofing comes to improve directly under the gate electrode 21.
[0026] in addition -- an example -- the single crystal substrate 11 -- Ga As although constituted -- especially -- Ga As not only -- it is applicable to a general semi-conductor, such as Si, germanium, and In P. Moreover, the impurity atom which carries out a delta dope is Si shown in the example. It does not restrict.
[0027] Moreover, it is also possible to consider as the structure which excluded the barrier layer 13 in the structure shown by drawing 1 , and it can also consider as the structure which excluded the barrier layer 16. The effectiveness that the temperature characteristic is improved also in the any is acquired. Moreover, i-aluminum Ga As which constitutes a barrier layer 16 and the cap layer 17, respectively A layer and i-Ga As It can also consider as the structure where face constituting a layer in n mold and constituting a field effect transistor, and an ion implantation is not performed.
[0028]
[Effect of the Invention] According to the compound semiconductor equipment applied to this invention as mentioned above, a transistor applicable to the high speed and high frequency circuit which do not have change in transistor characteristics, such as electron mobility, over a large temperature requirement can be constituted now.

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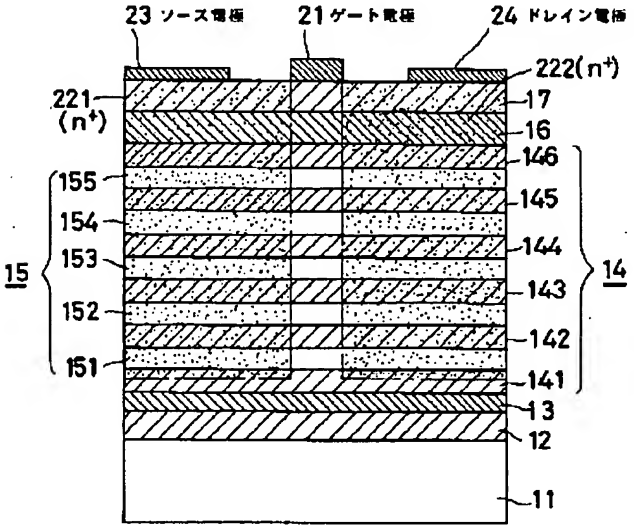
Drawing selection Representative drawing



11：半絶縁性GaAs基板
12：バッファ層（i-GaAs）
13：i-AlGaAs層
14：i-GaAs層
15：Siドーピング層
16：i-AlGaAs層（バリア層）
17：i-GaAs層（キャップ層）

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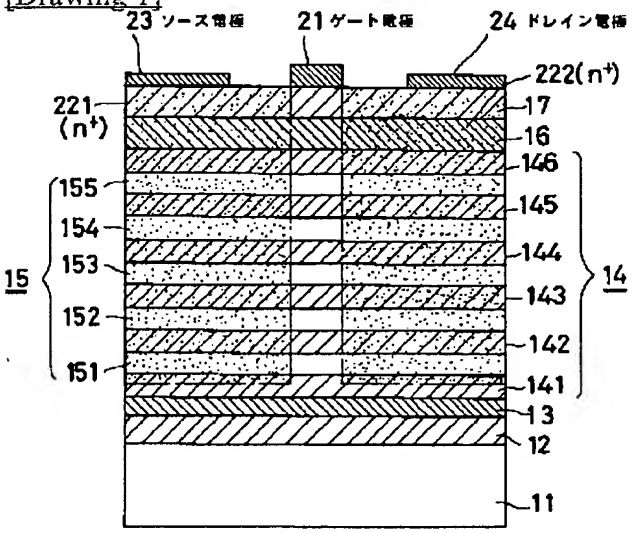
DRAWINGS

[Drawing 1]



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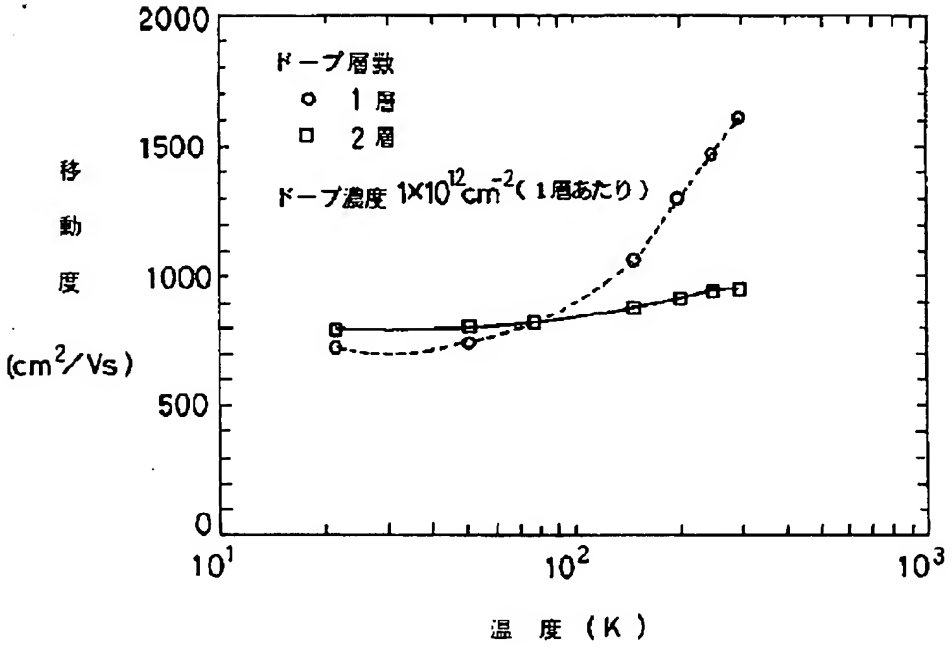
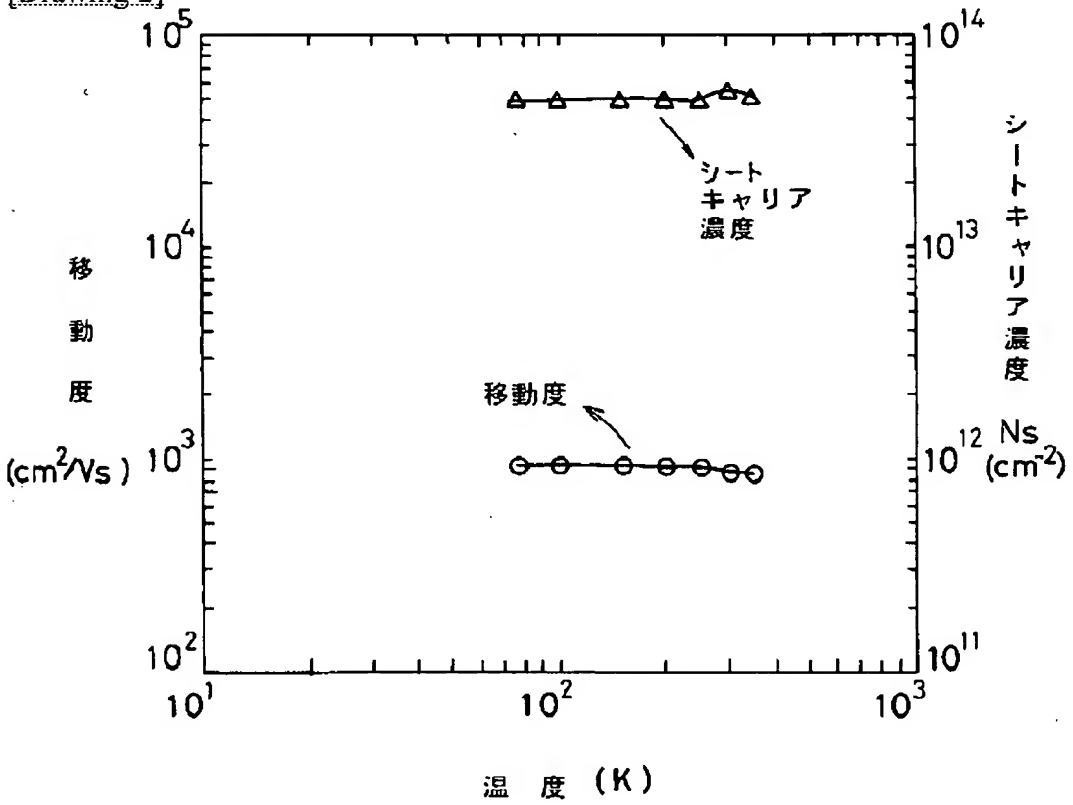
17：i-GaAs 層（キャップ層）

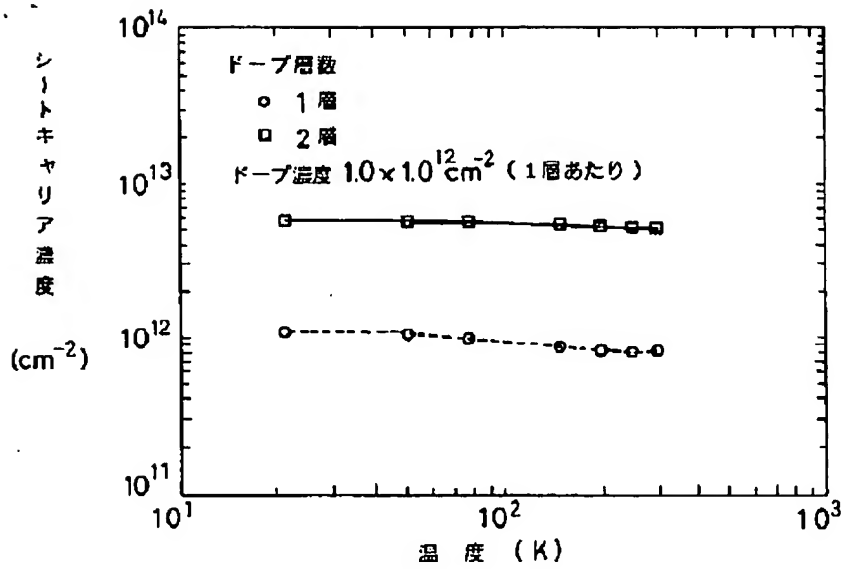
[Drawing 3]



[Drawing 2]



[Drawing 4]



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